REMARKS

Claims 1, 3-11, and 13-38 are pending. Claims 11, 20 and 32 have been amended. The Examiner objected to claim 32 and rejected claims 1, 3-11 and 13-38.

The Examiner objected to claim 32 as being grammatically incorrect. The Examiner is thanked for suggesting a correction. Applicants have amended claim 32 in accordance with the Examiner's suggestion. No change in claim scope is intended. Claims 11 and 20 have been amended to clarify their meaning. No change in claim scope is intended.

The Examiner rejected claims 1, 5, 10-11, 15, 20, 30-33 and 37-38 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,521,979 issued to Deiss. Applicants respectfully traverse the Examiner's contention that Deiss is an anticipating reference.

The Examiner also rejected claims 6-7, 16-17 and 34-36 under 35 U.S.C. § 103(a) as obvious over Deiss, without citing a second reference. The Examiner rejected claims 1, 3-11 and 13-20 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,959,659 issued to Dokic et al in view of ADSP-2100 Family User's Manual – Chapter 4: Data Transfer (the "Manual"). Finally, the Examiner rejected claims 21-38 under 35 U.S.C. § 103(a) as obvious over Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter, et al.

With regard to the merits, the Examiner has interpreted the claimed memory and data structures as including buffers in the circuitry for receiving the digital data stream. As an initial matter, Applicants respectfully submit that the Examiner is not interpreting the claims in accordance with MPEP 2111. The Examiner is required to give the claims the broadest reasonable interpretation consistent with the specification. The broadest reasonable interpretation of the claims must also be consistent with the interpretation those of skill in the art would reach.

Here, the Examiner has interpreted "a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the circuitry for receiving the digital data stream" wherein "control information" is retrieved from an "address in the memory" (see claim 1) as being disclosed by combinations of various components from the cited references, in each case including a component that is in the circuitry for receiving the digital data stream. For example, in the Examiner points to the memory 18 in Deiss that is

clearly part of the circuitry for receiving the digital data stream. *See, e.g.*, Deiss at column 1, lines 4-8 ("with emphasis on utilizing a common transport buffer memory"); column 4 at 11-23 ("The exemplary system of FIG. 3, first routes the respective packets to predetermined memory locations in the memory 18"). Similarly, the Examiner has in effect interpreted the claimed memory as being disclosed in part by packet buffers 200/202 of Dokic, which, according to the Examiner, is where the control information is stored prior to being transferred to the host processor. The packet buffers 200/202, however, are part of the circuitry for receiving the data stream.

The Examiner's interpretation is neither reasonable nor consistent with the interpretation that the claims would be given by one of skill in the art, as discussed in more detail below.

Deiss is Not An Anticipating Reference

As noted above, the Examiner rejected claims 1, 5, 10-11, 15, 20, 30-33 and 37-38 as anticipated by Deiss. Applicants respectfully traverse the Examiner's contention that Deiss is an anticipating reference.

Claims 1 and 10 recite "a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the circuitry for receiving the digital data stream ... a second control circuit for extracting a packet identifier from a data packet in the digital data stream ... a third control circuit for receiving the extracted packet identifiers and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier." Similarly, claims 11 and 20 recite "a memory separate from the data stream ... outputting, responsive to a match, an address in the memory ... accessing ... the address in memory [and] retrieving control information ... stored at such address."

The Examiner points to programmable signal component identifier ("SCID") registers 13 and memory 18 of Figure 3 of Deiss as the claimed memory, forward error correcting ("FEC") decoder 12, decrypter 16, header and e-code decoder 30 and smart card 31 as

the claimed second control circuit, and SCID match detector 15 and memory controller 17 as the claimed third control circuit, as well as the specification of Deiss at column 4, lines 40-67 and column 5, lines 30-33.

Deiss discloses signal component identifiers (SCID) which are stored in programmable registers (13). The SCIDs of received signal packets are compared with all the SCIDs in the programmable SCID registers. Responsive to a match the corresponding packet payload is stored in the appropriate memory area or block in memory 18, which is thus part of the circuitry for receiving the digital data stream. The Examiner appears to be suggesting that the apparatus disclosed by Deiss accesses the programmable registers (13) after a match has been found, in order to retrieve associated encryption information to decrypt the scrambled packet payload.

In fact, the packet decryption described by Deiss does not require any reference to the programmable registers 13. The packet header contains a CF field and a CS field. The field CF contains a flag to indicate whether the payload of the packet is scrambled, and the field CS contains a flag which indicates which of the two alternative unscrambling keys is to be utilized to unscramble scrambled packets. See column 3, lines 5 to 9. Only the signal payloads are scrambled and the packet headers are passed by the decryptor unaltered. Whether or not a packet is to be descrambled is determined by the CF flag in the packet prefix, and how it is to be descrambled is determined by the CS flag. If no SCID match is made for a respective packet, the decryptor may simply be disabled from passing any data. See column 4, lines 47 to 55. Further, the decryptor is programmed with decryption keys provided by the smart card apparatus 31. The smart card apparatus 31 is not the programmable SCID register 13 and as such, at no stage during the decryption of the packet does the apparatus disclosed by Deiss access the programmable SCID register 13. The CF and CS fields are not part of the SCID field and are therefore not stored in the programmable SCID register 13. See column 3, lines 2 to 5.

Thus, Deiss does not disclose "outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier" or "outputting, responsive to a match, an address in the memory ... accessing ... the address in memory [and] retrieving control

information ... stored at such address" as recited. Accordingly, Applicants respectfully submit that Deiss does not anticipate claims 1, 5 (which depends from claim 1), 10-11, 15 (which depends from claim 11) and 20.

Claim 30 recites "storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure." Claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

The Examiner points to the memory 18 as the first data structure and the SCID registers 13 and the memory controller 17 as the claimed second data structure. There is no indication or suggestion in Deiss that addressing information is stored in the SCID registers 13 or the memory controller 17, or that any addressing information (whether stored in SCID register 13 or otherwise) is outputted and used to retrieve control information from the memory 18. Thus Deiss does not disclose or suggest "outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" as recited. Claims 31-33 and 37 depend from claim 30. Accordingly, Applicants respectfully submit that claims 30-33 and 37-38 are not anticipated by Deiss.

Deiss Is Not An Appropriate Primary Reference

The Examiner rejected claims 6-7, 16-17 and 34-36 as rendered obvious by Deiss. Applicants respectfully traverse the Examiner's contention that Deiss renders any of the claims obvious. Claims 6-7 depend from claim 1, claims 16-17 depend from claim 11 and claims 34-35 depend from claim 30. (Applicants note that claim 7 depends from claim 3, against which the Examiner has not cited Deiss). The Examiner did not cite a secondary reference, and thus has not claimed that the teachings discussed above and missing from Deiss are disclosed or taught by

another reference. Accordingly, Applicants submit that claims 6-7, 16-17 and 34-35 are not rendered obvious by Deiss for the same reasons that claims 1, 11 and 30 are not anticipated by Deiss.

Dokic Is Not An Appropriate Primary Reference

The Examiner rejected claims 1, 3-11 and 13-20 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,959,659 issued to Dokic et al in view of ADSP-2100 Family User's Manual – Chapter 4: Data Transfer (the "Manual"). Applicants respectfully traverse the Examiner's contention that Claims 1, 3-11 and 13-20 are obvious over Dokic in view of the Manual.

As noted above, claims 1 and 10 recite "a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the circuitry for receiving the digital data stream ... a second control circuit for extracting a packet identifier from a data packet in the digital data stream ... a third control circuit for receiving the extracted packet identifiers and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier." Similarly, claims 11 and 20 recite "a memory separate from the data stream ... outputting, responsive to a match, an address in the memory ... accessing ... the address in memory [and] retrieving control information ... stored at such address."

The Examiner correctly identifies memory 205 as storing a PID filtering table. However, the Examiner goes on to assert that the buffers 200, 202 may store control information such as the program map table (PMT) or the program association table (PAT) as part of the data stream. Whether this is true or not is immaterial, as the Examiner has not identified the buffers 200, 202 as part of the claimed memory, and, as discussed below, the buffers store the data stream and thus cannot be part of the claimed memory. The claims recite that the "address" that is accessed to retrieve the control information is in the same "memory" in which the packet identifiers are stored and further, that this memory is "separate from the circuitry for receiving

the digital data stream." The claim language additionally requires that "the control information" is stored in and retrieved from the claimed "memory", as described above. Thus, the Examiner's assertion that the limitation pertaining to "control information" is not so limiting as to exclude for example the program map table (PMT) or program association table (PAT) is irrelevant.

The Examiner makes an alternative argument, stating that the packet header may contain timing information (PCR) which could be construed as control information, and that this control information is stored in the packet buffers, which the Examiner alternatively refers to as "the memory." Dokic states at column 8 lines 1 to 6: "transport packet buffers 200 and 202 are used to load transport packets from the MPEG-2 transport stream. Preferably, each buffer is 188 bytes long so that the buffer may contain an entire MPEG-2 transport packet. The buffers are loaded in a circular fashion, such that when one buffer is loading, the other buffer is being processed by a controller 204 within the digital signal processor." Thus, the packet buffers cannot be the claimed memory because they are not "separate from the circuitry for receiving the digital data stream" as recited.

For the reasons set forth above, Dokic is not an appropriate primary reference for claims 1, 3-11 and 13-20.

Further, the Examiner admits that Dokic does not disclose or suggest "outputting an address", but claims this is suggested by the Manual, which describes the operation of a circular buffer. The problem with this argument is that the circular buffer of Dokic that the Examiner suggests combining with the Manual is the circular buffer 200/202/205, which the Examiner admits stores the "entire packet" and which as discussed above cannot be the claimed memory because it is not "separate from the circuitry for receiving the digital data stream" as recited. Accordingly, Applicants respectfully submit claims 1, 3-11 and 13-20 are not rendered obvious by Dokic taken in combination with the Manual.

The Examiner also rejected claims 21-38 under 35 U.S.C. § 103(a) as obvious over Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter, et al. Applicants respectfully traverse the Examiner's contention that claims 21-38 are obvious over Dokic in view of Blatter.

Claims 21 and 29 recite "a first data structure for storing addressing information that is accessed based on packet identifiers ... a second data structure for storing control

information that is accessed based on addressing information extracted from the first data structure ... outputting addressing information responsive to a match ... wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information." Similarly, claim 30 recites ""storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" and claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

As an initial matter, the Examiner does not contend that Dokic or Blatter disclose or suggest "outputting" addressing information "responsive to a match" as claimed, and appear to expressly admit this is not disclosed or suggested by Dokic. For this reason alone, claims 21-38 are not rendered obvious by the combination of Dokic and Blatter.

Further, the Examiner admits that Dokic does not disclose or suggest the claimed first and second data structures. The Examiner points to unit 45 of Blatter as the first data structure of claims 21 and 29 and smart card system 130 as the second data structure of claims 21 and 29. The Examiner does not identify how to combine unit 45 and smart card system 130 with Dokic so as to achieve the claimed invention. In any event, there is no indication or suggestion in the cited portion of Blatter that smart card system 130 is accessed based on addressing information extracted from unit 45. In Blatter, encryption keys are generated by smart card system 130 based on codes in the input data stream and preloaded into unit 45. *See* Blatter at column 5, lines 8-14. Thus, neither Dokic nor Blatter teach or suggest "a second data structure for storing control information that is accessed based addressing information extracted from the first data structure" as recited in claims 21 and 29. Moreover, while the encryption keys may be considered "control information", there is no motivation to "retrieve" the keys from smart card 130 because they are preloaded into unit 45. Nor is there any motivation to output "addressing

information." For similar reasons, neither Dokic nor Blatter teach or suggest "retrieving ... based on the outputted addressing information, control information" as recited in claims 30 and 38.

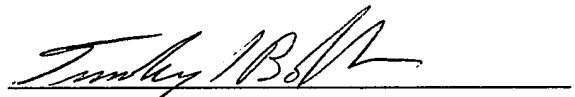
Claims 22-28 depend from claim 21 and claims 31-37 depend from claim 30. Accordingly, Applicants submit that claims 21-38 are not rendered obvious by Dokic in view of Blatter.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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